Fabrication of Graphene Moiré Superlattice Devices

2023 GQL IRTE Intern: Desvaun Drummond

2023 GQL IRTE Intern Affiliation: Electrical Engineering, Howard University

2023 GQL IRTE Principal Investigator: Dr. Takuya Iwasaki

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Contact: desvaun@gmail.com, iwasaki.takuya@nims.go.jp

Website: https://cnf.cornell.edu/education/reu/2023

Abstract:

Graphene, a two-dimensional (2D) sheet with carbon atoms arranged in a honeycomb lattice, has attracted attention because of its unique electronic properties. When graphene is stacked on hexagonal 2D materials such as graphene or hexagonal boron nitride (hBN), an interference pattern (moiré pattern) emerges in the stacking structure due to a small lattice constant mismatch or rotational misalignment. This moire superlattice has a long-period structure, giving rise to intriguing emergent properties in the materials beyond the original band structure of parent layers. To utilize such properties for device applications, investigation of fundamental properties in moiré superlattices should be imperative.

Summary of Research:

Graphene and hBN were grown from exfoliating kish graphite and hBN flakes using scotch tape. An original transfer station was used to assemble the graphene/hBN heterostructures, and an atomic force microscopy (AFM) was used to scan the heterostructure. A viscoelastic polymer stamp is required for the transfer process, as it minimizes the possible contamination of graphene. Figure 1 shows the final stamps to be used for assembling the heterostructure.

Once the heterostructures are fabricated using the transfer station, thermal annealing was carried out in a vacuum chamber with argon as a protection gas, and at an elevated temperature of 400°C. This process helps to reduce the bubbles around the surface of the graphene in the heterostructure. Bubbles should be avoided as they can degrade the electronic transport property and the device performance by acting as charge traps or scattering centers. The completed heterostructure after annealing is showed in Figure 2, where the outline of graphene can be seen in the middle of the heterostructure.

After annealing, the graphene field effect transistor was fabricated in the NIMS Sengen cleanroom using techniques such as electron-beam lithography, reactive ion etching, and photoresist coating. The device was designed using AutoCAD, where contact electrodes, pads, and Hall bar were outlined in order to test the electrical response of the device after fabrication. The final structure after fabrication is showed in Figure 3, where two devices were placed on the heterostructure.

The final step of the project was to demonstrate the evidence of graphene in the device by testing the device mobility. Using a probe station at room temperature, as shown in Figure 4, this tool can measure the electrical characteristics of a device and confirm the presence of graphene. Additionally, the Keysight B2901A precision source / measure unit (SMU) was used with the probe station. This tool is a 1-channel, compact, and cost-effective benchtop SMU with the capability to source and measure both voltage and current.

Conclusions and Future Steps:

Our results proved consistent with the standard mobility of graphene. However, the mobility of Device A was much lower than Device B. The exact cause of this difference is unknown, but we were still able to demonstrate evidence of graphene's ambipolar characteristics and high carrier mobility and we fabricated high-quality heterostructure devices for this experiment. Future steps are to test the device at low temperature, around 1.5 K, and perform quantum hall effect measurements.

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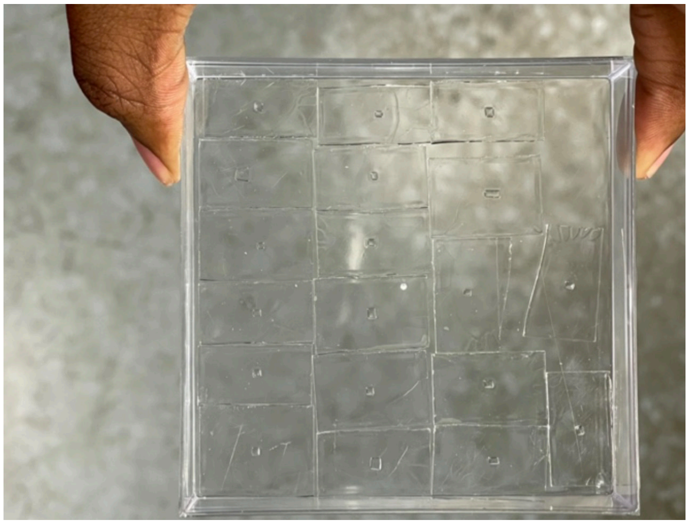

Figure 1: Viscoelastic polymer stamps.

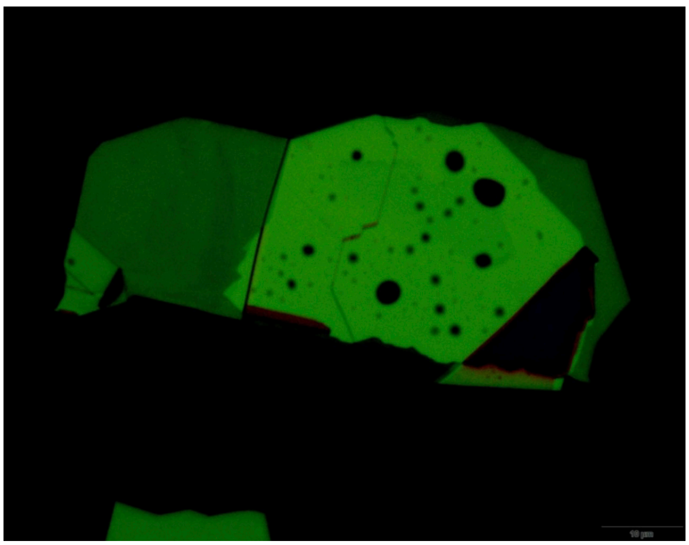

Figure 2: Image of fabricated graphene/hBN heterostructure after thermal annealing.

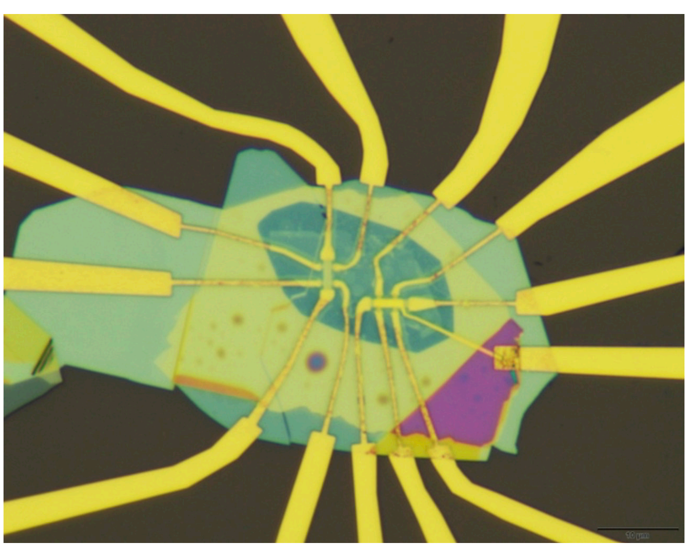

Figure 3: Fabricated graphene FET device.

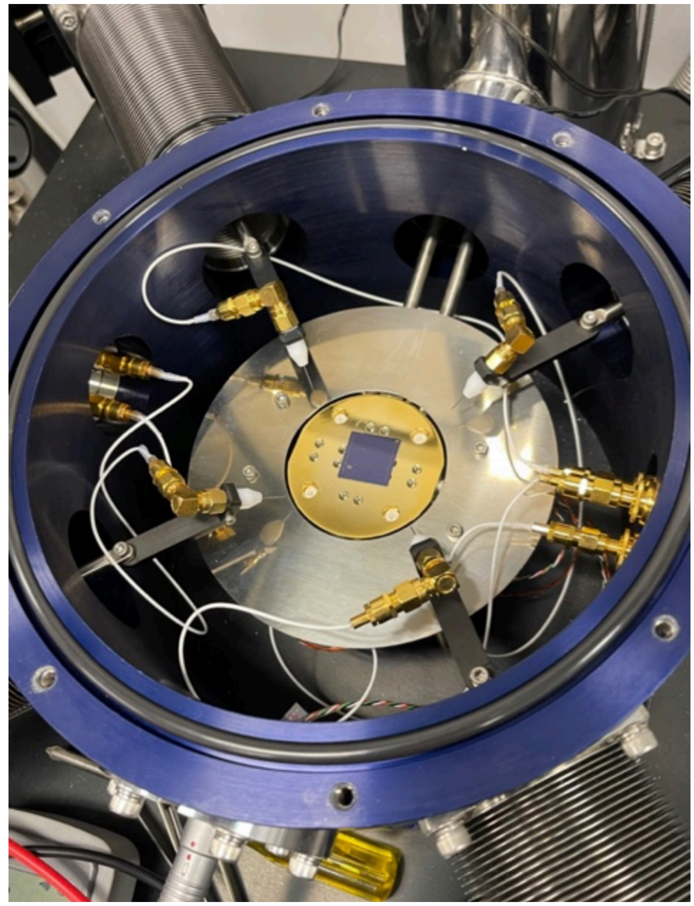

Figure 4: Probe station.

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